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Substitute for form 1448A/PTO				Complete if Known	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				Application Number	0 / 726 005
				Filing Date	December 1, 2003
				First Named Inventor	Crocidisso Marco Antonio Renna
				Art Unit	2813
				Examiner Name	
Sheet	1	of	2	Attorney Docket Number	2110-91-3

[illegible][illegible]

Examiner Signature	<i>James A. Quinn</i>	Date Considered	10/13/05
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 601.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6 Applicant is to place a check mark here if English language translation is attached.

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Sheet 2 of 2	Attorney Docket Number	2110-91-3	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
MDH		European Search Report for 02425742.0 dated August 6, 2003	
↓		Tsunashima, et al. "A New Substrate Engineering Technique to Realize Silicon on Nothing" Electrochemical Society Proceedings, Electrochemical Society, Pennington, NJ, US, No. 17, 2000, pp. 532-546, XP008004134 ISSN: 0181-4374	
↓		Sato, et al. "SON (silicon on nothing) MOSFET Using ESS (empty space in silicon) Technique for SoC Applications" International Electron Devices Meeting 2001. IEDM. Technical Digest, Washington, DC, Dec. 2-5, 2001, New York, NY: IEEE, U.S., 2 December 2001, pp. 3771-3774, XP010575245 ISBN: 0-7803-7050-3	

Examiner Signature	<i>Marco D. Renna</i>	Date Considered	10/13/05
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